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09/632,521	08/04/2000	Efstathios Papaefstathiou	205102	1492

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	4

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,521	PAPAEFSTATHIOU, EFSTATHIOS	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 have been examined and claims 1-31 have been rejected.

Priority

2. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. The provisional application number is 60/209,759, filed June 6, 2000.

Abstract

3. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Specification

4. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

4-1. It appears that "output peripheral interface 190", as described in line 13 of page 11, should be "output peripheral interface 195".

4-2. It appears that "evaluation engine 220", as described in line 4 of page 16, should be "evaluation engine 202".

4-3. It appears that "hardware and model configuration APIs", as described in lines 12-13 of page 25, should be "hardware model APIs".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-7, 10-14, 16-17, 20-24, 26-27, and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Papaefstathiou et al., "An Introduction to the Layered Characterisation for High Performance Systems", Research Report CS-RR-335, The University of Warwick, December 5, 1997.

6-1. Regarding claim 1, Papaefstathiou et al. disclose a method for executing a computer system performance analysis (PACE toolset, Abstract), the method comprising the steps of:

first providing a workload specification comprising a set of resource uses (resource usage, page 3, paragraph 3);

second providing at least one hardware model, independently defined with regard to the workload specification, comprising hardware performance information (hardware layer, page 2, paragraph 7, bullet 4);

third providing a configuration defining system components and including a reference to the hardware model (parallelisation template, page 2, paragraph 7); and

applying the configuration to the workload specification to render performance data, wherein the applying step comprises referencing the hardware model to render hardware performance information corresponding to an event derived from the set of resource uses (evaluation engine, page 3, paragraph 2).

6-2. Regarding claim 2, Papaefstathiou et al. further disclose the third providing step comprises:

creating the configuration from a script independently designated with respect to the workload specification (special purpose language scripts, page 2, paragraph 8, bullet 1).

6-3. Regarding claim 3, Papaefstathiou et al. further disclose comprising the step of:

providing an extensible schema defining a set of syntactic rules under which the script is formulated (rules that govern this relationship, page 5, paragraph 1).

6-4. Regarding claim 4, Papaefstathiou et al. further disclose comprising extending the set of syntactic rules according to definitions specified for the hardware model (defined in a hardware symbol file, page 5, last paragraph).

6-5. Regarding claim 6, Papaefstathiou et al. further disclose the hardware performance information comprises a modeled delay associated with an identified event (execution time, page 8, paragraph 4).

6-6. Regarding claim 7, Papaefstathiou et al. further disclose the identified event comprises a communication event (inter-processor communication, page 8, paragraph 4).

6-7. Regarding claim 10, Papaefstathiou et al. further disclose comprising the steps of:

providing a set of user-specifiable instructions for controlling evaluation of a sub-set of a list of events associated with a workload specification (user will be able to edit his/her own PACE language scripts, page 3, paragraph 4).

6-8. Regarding claim 11, Papaefstathiou et al. disclose a performance technology infrastructure facilitating integrating independently designated workload and hardware

descriptions in a performance analysis (PACE toolset, Abstract), the performance technology infrastructure comprising:

a workload specification interface; a hardware model interface (Object interfacing, page 5, Figure 3);

a component configuration (parallelisation template, page 2, paragraph 7) database; and

an evaluation engine comprising an augmentable program structure (the interface includes the external variables that can be modified outside of the object scope, page 4, last paragraph) including:

a set of slots for receiving a workload specification via the workload specification interface, and a component configuration from the component configuration database, wherein hardware model performance data corresponding to devices specifiable within the component configuration is retrieved from at least one hardware model via the hardware model interface (evaluation engine, page 3, paragraph 2).

6-9. Regarding claim 12, Papaefstathiou et al. further disclose the component configuration is specified in the form of a script, and wherein the script is independently designated with respect to the workload specification (special purpose language scripts, page 2, paragraph 8, bullet 1).

6-10. Regarding claim 13, Papaefstathiou et al. further disclose comprising an extensible configuration schema defining a set of syntactic rules under which the script is formulated (rules that govern this relationship, page 5, paragraph 1).

6-11. Regarding claim 14, Papaefstathiou et al. further disclose comprising a program architecture facilitating extending the set of syntactic rules according to definitions specified for the hardware model (defined in a hardware symbol file, page 5, last paragraph).

6-12. Regarding claim 16, Papaefstathiou et al. further disclose the hardware performance information comprises a modeled delay associated with an identified event (execution time, page 8, paragraph 4).

6-13. Regarding claim 17, Papaefstathiou et al. further disclose the identified event comprises a communication event (inter-processor communication, page 8, paragraph 4).

6-14. Regarding claim 20, Papaefstathiou et al. further disclose comprising:

a set of user-specifiable instructions for controlling evaluation of a sub-set of a list of events associated with a workload specification (user will be able to edit his/her own PACE language scripts, page 3, paragraph 4).

6-15. Regarding claims 21-24, 26-27, and 30, these medium claims include equivalent method limitations as in claims 1-4, 6-7, and 10, and are anticipated using the same analysis of claims 1-4, 6-7, and 10.

6-16. Regarding claim 31, Papaefstathiou et al. disclose a performance technology infrastructure facilitating integrating independently designated workload and hardware descriptions in a performance analysis (PACE toolset, Abstract), the performance technology infrastructure comprising:

a workload specification interface; a hardware model interface (Object interfacing, page 5, Figure 3);

a component configuration (parallelisation template, page 2, paragraph 7) database; and

an evaluation engine including a set of slots for receiving a workload specification via the workload specification interface, and for receiving a component configuration from the component configuration database, wherein hardware model performance data corresponding to

devices specifiable within the component configuration is retrieved from at least one hardware model via the hardware model interface (evaluation engine, page 3, paragraph 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 15, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papaefstathiou et al., "An Introduction to the Layered Characterisation for High Performance Systems", Research Report CS-RR-335, The University of Warwick, December 5, 1997, in view of Brooke et al., U.S. Patent 6,748,569 B1 issued June 8, 2004, and filed September 20, 1999.

8-1. Regarding claims 5, 15, and 25, Papaefstathiou et al. disclose a method for executing a computer system performance analysis (PACE toolset, Abstract) wherein the step comprises creating the configuration from a script independently designated with respect to the workload specification (special purpose language scripts, page 2, paragraph 8, bullet 1). However, Papaefstathiou et al. fail to disclose expressly the configuration comprises an XML script.

Brooke et al. disclose "XML enables users to create unique tags that identify their information in more meaningful ways than simply applying a basic set of markup language tags to all documents" (column 6, lines 26-28) as well as a method for generating XML documents using a script language that extends the capabilities of XML (Abstract). In other words, the script language and script processor provide facilities for gathering content and style information

from a plurality of sources (Abstract). An example of an XML script source file is shown in Fig. 5.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Papaefstathiou et al. to incorporate the teachings of Brooke et al. to obtain the invention as specified in claims 5, 15, and 25 because it will extend the capabilities of XML and provide facilities for gathering content and style information from a plurality of sources in more meaningful ways.

9. Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papaefstathiou et al., "An Introduction to the Layered Characterisation for High Performance Systems", Research Report CS-RR-335, The University of Warwick, December 5, 1997, in view of Papaefstathiou et al., "A Common Workload Interface for the Performance Prediction of High Performance Systems", IEEE Int. Symp. on Computer Architecture, Workshop on Performance Analysis in Design (PAID'98) June, 1998.

9-1. Regarding claims 8, 18, and 28, Papaefstathiou et al. disclose a method for executing a computer system performance analysis (PACE toolset, Abstract). However, Papaefstathiou et al. fail to disclose expressly rendering an output trace. Nevertheless, Papaefstathiou et al. suggest the main components of the PACE toolset include "a further set of graphical interface tools that allow the user to define aspects of the performance study and visualize the outputs" at page 3, first paragraph.

In their PAID'98 paper, Papaefstathiou et al. disclose "the most commonly output facility is the creation of predictive trace files. These are analogous to traditional trace obtained at run-time but contain predicted time information" (page 4, right column, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Papaefstathiou et al. to incorporate the teachings of Papaefstathiou et al. in their PAID'98 paper to obtain the invention as specified in claims 8, 18, and 28 following the suggestion of Papaefstathiou et al.

10. Claims 9, 19, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Papaefstathiou et al., "An Introduction to the Layered Characterisation for High Performance Systems", Research Report CS-RR-335, The University of Warwick, December 5, 1997, and "A Common Workload Interface for the Performance Prediction of High Performance Systems", IEEE Int. Symp. on Computer Architecture, Workshop on Performance Analysis in Design (PAID'98) June, 1998, as applied to claims 8, 18, and 28, in view of Brooke et al., U.S. Patent 6,748,569 B1 issued June 8, 2004, and filed September 20, 1999.

10-1. Regarding claims 9, 19, and 29, Papaefstathiou et al. disclose a method for executing a computer system performance analysis (PACE toolset, Abstract) comprising rendering an output trace. However, Papaefstathiou et al. fail to disclose expressly that output trace formats are specified by XML schemas.

Brooke et al. disclose, "A schema specifies the structure of an XML document and constraints on its content. XML defines rules for defining markup languages having tags, while a schema is a formal specification of the grammar for one markup language. A schema is useful for validating the document content and for describing the grammar of the language. The schema defines the elements that can appear within the document and the attributes that can be associated with an element. XML schemas are extensible and software developers are free to add their own elements and attributes to XML schema documents" (column 6, lines 55-65). In

other words, when output trace formats are specified by XML schemas, software developers are free to add their own elements and attributes to present the output trace.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Papaefstathiou et al. to incorporate the teachings of Brooke et al. to obtain the invention as specified in claims 9, 19, and 29 because software developers are free to add their own elements and attributes to present the output trace.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to McDonald et al., U.S. Patent 5,881,268 issued March 9, 1999, is cited as disclosing a performance modeling tool and method.

Reference to Abu El Ata, U.S. Patent 6,311,144 B1 issued October 30, 2001, and filed July 31, 1998, is cited as disclosing an information design system using multi-layer mathematical models.

Reference to Yang et al., U.S. Patent 6,542,854 B2 issued April 1, 2003, and filed April 30, 1999, is cited as disclosing a method for profiling a system.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean Homere can be reached on (703) 308-6647. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day H.D.
September 20, 2004

JEAN B. HOMERE
PRIMARY EXAMINER